PATENT

In the Specification

Paragraph 32

An implant sequence is carried out so that portions thereof can serve as one of the plates of the storage capacitor. Specifically, an implant mask is first applied such that portions of the rails are masked except those that are within the region Cst1 as shown in Fig. 2. The implant mask can be a layer of silicon nitride that is deposited and then etched through a photolithographic mask, or it could be a photolithographic mask itself. Then a low energy, high concentration implant is carried out to render the exposed portions of the rails conductive. Phosphorous, boron, arsenic, or any other conductivity-enhancing implant could be used. A phosporus implant is preferred, at a concentration in the range of 1 times 10 to the 20th power per centimeter cubed (abbreviated as $\underline{1 \times 10^{20} cm^{-3}}$ ~~1x10E20/cm3)~~ and an energy in the range of 1 to 3 kilovolts (kev) and is typically angled 30 to 45 degrees off of the axis perpendicular to the wafer plane and at four or more orientations of the wafer in order to ensure that all orientations of fins receive sufficient ion dose. Note that the concentration and energy of this implant is equal to or greater than that subsequently utilized to form the source/drain diffused electrodes of transfer devices TR1, TR2.